REMARKS/ARGUMENTS

Claims 1, 3-12, 14-24, 26-27 and 29-38 stand rejected under 35 U.S.C. §102(e) as being anticipated by United States Patent No. 6,000,004 to Fukumoto (the "Fukumoto reference"). For at least the following reasons, Applicants respectfully submit that the Fukumoto reference does not anticipate Claims 1, 3-12, 14-24, 26-27 and 29-38.

Claim 1 recites:

> A method of programming information in a memory arrangement of a computer, comprising the steps of:
> providing an identifier into an area of the memory arrangement that is to be programmed, the identifier identifying a correct programming of the memory arrangement; and
> altering the identifier in the memory arrangement before programming the information.

In support of the rejection, the Examiner contends that the "block protect indicator taught by Fukumoto indicates **a correct programming** and erasing ***area*** by indicating that **programming** and erasing **is allowed** to the corresponding region (C 11, L 7-11)." (Office Action, p. 5, "Response to Arguments" section). Applicants note that the Examiner is once again reverting to the claim interpretation previously raised in the Advisory Action mailed on March 5, 2003, i.e., the Examiner essentially contends that the phrase "correct programming of the memory arrangement" means "an approved area to program." However, the Examiner's interpretation is incorrect for at least two reasons. First, in contrast to the Examiner's interpretation, claim 1 does not recite that the identifier identifies a correct programming ***area***; rather, claim 1 clearly recites that the identifier identifies "a **correct programming** of the memory arrangement." Second, the Examiner's interpretation clearly contradicts the meaning of the phrase "a **correct programming** of the memory arrangement" as described in the specification. The second issue will be explained in further detail below.

During patent examination, the pending claims must be interpreted in a manner "***consistent with the specification***." MPEP 2111. Reading a claim ***in light of the specification***, to thereby interpret limitations explicitly recited in the claim, is a quite different thing from reading limitations of the specification into a claim, to thereby narrow the scope of

the claim. MPEP 2111. In addition, the broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. MPEP 2111. Furthermore, "Applicant may be his or her own lexicographer as long as the meaning assigned to the term is not repugnant to the term's well known usage." MPEP 2111.01.

The meaning of the phrase "a correct programming of the memory arrangement" is clearly described throughout Specification to be consistent with the interpretation asserted by Applicants, i.e., ***programming operation has been completed correctly in the memory arrangement***. For example, the Specification indicates the following:

> The method and the respective device serve to secure the functionality of a control unit, for example, when an interruption or malfunction has occurred during erasing and/or programming. To do so, when an interruption or a reset occurs during erasing or programming or when the device otherwise becomes de-energized, this is noted in a memory device, in particular in the memory device to be programmed. **In addition, in programming an identifier that identifies correct erasing and/or programming of the memory is entered into an area of the memory that is to be erased and/or programmed later**, in particular an area that is to be erased and/or programmed last, **and this identifier is altered before erasing or programming the data or programs in such a way that the program is not executed if programming is incomplete and/or the data is not used if data entry is not complete.** Thus, an error in programming or erasing can be corrected after a possible data modification.
>
> Advantageously, **the expected identifier that identifies the completeness and accuracy of the programming** is used as part of the program, in particular as part of the program identifier itself, and consequently does not take up any additional memory. (Specification, p. 3, l. 23 - p. 4, l. 6, *emphasis added*).

Thus, when viewed in light of the Specification, it is clear that the phrase "correct programming" as used in the present application means that a programming operation has been completed correctly, not "an approved area to program" as asserted by the Examiner.

In view of the above explanation, it is quite clear that the block protect (BP) storage region and the erase complete (EC) storage region described in the Fukumoto reference do not teach or suggest "providing an **identifier** into an area of the memory arrangement that is to be programmed, the **identifier identifying a correct programming** of the memory arrangement," as recited in claim 1. The BP storage region is provided "in order to protect the data stored in

each block. In this case, if the BP data is stored in the BP data storage region, then the erase and the write of the data from/into the block are prohibited in principle." Fukumoto, col. 4, ll. 40-43. Furthermore, the section of Fukumoto cited by the Examiner, col. 11, l. 7-11, merely indicates that "the BP data storage region 1a disables the erase and the write of data from /into the block 1 (to which the region 1a belongs) and thereby protects the data stored therein, if the BP (block protect) data has been stored in the BP data storage region 1a." Thus, the BP data does not serve to identify a correct programming of the memory arrangement as claimed and described in the present specification, e.g., the above-quoted section of p. 3, l. 23 - p. 4, l. 6. In addition, the data in the EC storage area of Fukumoto is erased during an erase operation. Fukumoto, col. 14, ll. 9-11. After the erase operation is complete, the EC data is written to the EC storage area. Fukumoto, col. 14, ll. 11-13. The EC data is only rewritten during an erase operation. Fukumoto, col. 13-15. Thus, the EC storage data does not serve to identify a correct programming of the memory arrangement.

Independent claims 12, 24, and 27 recite features similar to the above-discussed feature of claim 1 regarding an identifier identifying a correct programming of the memory arrangement. For at least the reasons stated above, the Fukumoto reference does not disclose each and every feature recited in independent claims 1, 12, 24, and 27, as well as dependent Claims 3-11, 14-13, 26, and 29-32. It is therefore respectfully requested that this rejection be withdrawn.

Claim 33 recites:

> A method of erasing information in a memory arrangement of a computer, comprising:
>
> providing an identifier into an area of the memory arrangement that is to be erased, the identifier identifying a correct erasing of the memory arrangement; and
>
> altering the identifier in the memory arrangement before erasing the information.

The Fukumoto reference does not disclose "altering the identifier in the memory arrangement before erasing the information." According to the Fukumoto reference, the EC storage area is erased during the erase operation, and the data stored in the EC storage area is rewritten only when the erase operation is performed. Fukumoto, col. 14, ll. 9-15. However, the Examiner contends that the claimed feature of "altering the identifier in the memory

arrangement before erasing the information" is met by Fukumoto since "an identifier is altered **during a previous erase and/or programming operation**, which occurs before a current erase and/or programming operation." Applicants note that the Examiner's interpretation completely ignores the fact that the claimed feature of "altering the identifier in the memory arrangement before **erasing** the information" is preceded by the claimed feature that "identifier" identifies "a correct **erasing** of the memory arrangement," and the "erasing" recited in both of the claimed features refers to **the same step**.

In addition, and independent of the above, the Examiner's contention that the "**altering of BP during a previous erase or program operation**" as taught by Fukumoto satisfies the claimed feature of **"altering the identifier in the memory arrangement before erasing the information**" completely contradicts the Examiner's concurrent assertion that **BP** of Fukumoto **indicates** "that programming and erasing is allowed to the corresponding region," since "the **protected state is released by rewriting the BP data** stored in the BP data storage region" (col. 14, l. 5-7) **during a previous erase and/or programming operation** as alleged by the Examiner, which means the BP data storage region 1a **does not** provide the block protect function of disabling "the erase and the write of data from/into the block 1" (col. 11, l. 7-11) **for the current erase and/or programming operation**.

For the foregoing reasons, neither the BP storage data operation nor the EC storage data operation of Fukumoto teaches or suggests the claimed features of providing an "identifier" that identifies "a correct **erasing** of the memory arrangement," and "altering the identifier in the memory arrangement before **erasing** the information," as recited in claim 33. Since the Fukumoto reference does not disclose at least these features, the Fukumoto reference does not anticipate Claim 33. It is respectfully submitted that claim 33 is in condition for allowance.

Claim 34 recites a feature similar to the above-recited feature of claim 33 regarding altering the identifier before erasing the information. For at least the reasons described above in connection with claim 33, the Fukumoto reference does not anticipate new claim 34. It is respectfully submitted that claim 34 is in condition for allowance.

Claim 35 recites:

> A method of erasing and programming information in a memory arrangement of a computer, comprising:
> providing an identifier into an area of the memory arrangement that is to be erased and programmed, the identifier identifying a correct erasing and programming of the memory arrangement; and
> altering the identifier in the memory arrangement before erasing and programming the information.

As discussed above in connection with claim 33, the Fukumoto reference does not disclose an identifier identifying a correct programming of the memory arrangement, let alone disclose an "identifier identifying a correct erasing and programming of the memory arrangement" or "altering the identifier . . . before erasing and programming the information." For these reasons, the Fukumoto reference does not anticipate claim 35. It is respectfully submitted that claim 35 is in condition for allowance.

Claims 36-38 recite features similar to the feature of claim 35 regarding an identifier identifying a correct erasing and programming of the memory arrangement. For at least the reasons described above in connection with claims 33 and 35, the Fukumoto reference does not anticipate claims 36-38. It is respectfully submitted that claims 36-38 are in condition for allowance.

Claims 2, 13, 25 and 28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the Fukumoto reference. Claims 2, 13, 25, and 28 depend from Claims 1, 12, 24, and 27, respectively. Since the Fukumoto reference does not anticipate Claims 1, 12, 24 and 27 as described above, the Fukumoto reference cannot render dependent Claims 2, 13, 25, and 28 obvious under 35 U.S.C. §103(a). It is therefore respectfully requested that this rejection be withdrawn.

CONCLUSION

In light of the foregoing, Applicants respectfully submit that all of the pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully Submitted,

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